



Welcome United States Patent and Trademark Office

Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

SUPPORT

Results for "(((storage or disk or disc)<in>metadata) <and> (controller and virtual*<in>met..."

Your search matched 1 of 1328352 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.

e-mail printer friendly

» Search Options

[View Session History](#)
[New Search](#)

Modify Search

☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

 [Select All](#) [Deselect All](#)

- ☐ 1. **An efficient BIST method for distributed small buffers**
 Jone, W.B.; Huang, D.C.; Wu, S.C.; Lee, K.J.;
[Very Large Scale Integration \(VLSI\) Systems](#), IEEE Transactions on
 Volume 10, Issue 4, Aug. 2002 Page(s):512 - 515
 Digital Object Identifier 10.1109/TVLSI.2002.800532
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(288 KB\)](#) IEEE JNL
[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2006 IEEE -- All Rights Reserved





Welcome United States Patent and Trademark Office

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Sitemap](#) | [Help](#)

[AbstractPlus](#)

[View Search Results](#)

[Access this document](#)

Full Text: PDE (288 KB)

[Download this citation](#)

[Choose Citation & Abstract](#)

[Download ASCII Text](#)

[Learn More](#)

[Rights and Permissions](#)

[Learn More](#)

[BROWSE](#)

[SEARCH](#)

[IEEE Xplore GUIDE](#)

[SUPPORT](#)

[E-mail](#) [Twitter](#) [Facebook](#)

An efficient BIST method for distributed small buffers

Jone, W.B., Huang, D.C., Wu, S.C., Lee, K.J.

Dept. of Comput. Sci. & Inf. Eng., Nat. Chung-Cheng Univ., Chiayi, Taiwan

This paper appears in: *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*

Publication Date: Aug. 2002

Volume: 10, Issue: 4

On page(s): 512 - 515

ISSN: 1063-8210

INSPEC Accession Number: 7527810

Digital Object Identifier: 10.1109/VLSI.2002.800632

Posted online: 2003-02-19 12:48:59.0

Abstract

In this work, we propose a new built-in self-testing (BIST) method that is able to concurrently test a set of spatially distributed embedded-memory modules with different sizes. Using the concept of **redundant read-write** operations, we develop a new march method, called RSMarch, to efficiently test each memory module. The new method has the advantages of low hardware overhead, short test time, and high-fault coverage. The total test time is dominated by large-size modules. To further reduce the test time, we also propose a split-mode test method to **virtually** partition each large memory array into smaller modules, which can be tested simultaneously.

[Index Terms](#)

[Inspec](#)

Controlled Indexing

VLSI: [buffer storage](#) [built-in self test](#) [integrated circuit testing](#) [integrated memory circuits](#) [logic testing](#) [system-on-chip](#)

Non-controlled Indexing

BIST method [BSMarch](#) [SOC testing](#) [built-in self testing](#) [concurrent testing](#) [distributed small buffers](#) [high-fault coverage](#) [low hardware overhead](#) [march method](#) [redundant read-write operations](#) [serial interface technique](#) [short test time](#) [spatially distributed embedded-memory modules](#) [split-mode test method](#) [system-on-chip testing](#)

Author Keywords

Not Available

References

- 1 L. Temullo, R. D. Adams, J. Connor, and G. S. Koch, "Deterministic self-test of a high-speed embedded memory and logic processor subsystem," in *Proc. Int. Test Conf.*, 1995, pp. 33-44.
[Abstract](#) | Full Text: PDE (1308KB)

- 2 P. Mazunder and J. K. Patel, "Parallel testing for pattern-sensitive faults in semiconductor random-access memories," *IEEE Trans.*

Comput., vol. C-38, no. 3, pp. 394-407, Mar. 1989.
 Abstract | Full Text: EDE (1108KB)

3 T. Shridhar, "A new parallel test approach for large memories," *IEEE Des. Test Comput.*, vol. 3, pp. 15-22, Apr. 1986.
[Buy Via AskIEEE!](#)

4 Y. Morooka, S. Mori, M. Miyamoto, and M. Yamada, "An address maskable parallel testing for ultra high density drams," in *Proc. Int. Test Conf.*, 1991, pp. 556-563.
 Abstract | Full Text: EDE (764KB)

5 J. C. Lee, Y. S. Kang, and S. Kang, "A parallel test algorithm for pattern sensitive faults in semiconductor random access memories," in *Proc. Int. Symp. Circuit Systems*, 1997, pp. 2721-2724.
 Abstract | Full Text: EDE (364KB)

6 B. Nadeau-Dostie, A. Silburt, and V. K. Agarwal, "Serial interfacing technique for embedded memory testing," *IEEE Des. Test Comput.*, vol. 7, no. 2, pp. 52-63, Apr. 1990.
 Abstract | Full Text: EDE (784KB)

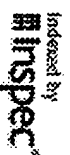
7 S. C. Wu, *A Parallel BIST Method for RAM-Based FIFO's*, Master Thesis, Taiwan: Dept. of Computer Science and Information Engineering, National Chung-Cheng University, 1997.

8 D. C. Huang, *Testing and diagnosis for distributed memory buffers*, Ph.D. dissertation Chiayi, Taiwan: Dept. of Computer Science and Information Engineering, National Chung-Cheng University, 2000.

Citing Documents

1 An efficient BIST method for non-traditional faults of embedded memory arrays, Jone, W.-B.; Der-Chen Huang; Das, S.R.
Instrumentation and Measurement, IEEE Transactions on
 On page(s): 1381- 1390, Volume: 52, Issue: 5, Oct. 2003
 Abstract | Full Text: EDE (412)

◀ [View Search Results](#)

Indexed by
 inspec

[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2006 IEEE. All Rights Reserved.

Refine Search

Search Results -

Terms	Documents
((storage or disk or disc) near5 controller) same virtual\$7 same redundant	7

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L1

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Friday, March 17, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

DB=DWPI; PLUR=YES; OP=OR

L1 ((storage or disk or disc) near5 controller) same virtual\$7 same redundant**Hit Count Set Name**

result set

7 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 and "point-to-point"	7

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L3

Search History

DATE: Friday, March 17, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L2 and "point-to-point"

L2 ((storage or disk or disc) near5 controller) same virtual\$7 same redundant

DB=DWPI; PLUR=YES; OP=OR

L1 ((storage or disk or disc) near5 controller) same virtual\$7 same redundant

Hit Count Set Name

result set

7 L3

138 L2

7 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 and "point-to-point"	0

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L4

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Friday, March 17, 2006 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 L2 and "point-to-point"

0 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 L2 and "point-to-point"

7 L3

L2 ((storage or disk or disc) near5 controller) same virtual\$7 same redundant

138 L2

DB=DWPI; PLUR=YES; OP=OR

L1 ((storage or disk or disc) near5 controller) same virtual\$7 same redundant

7 L1

END OF SEARCH HISTORY